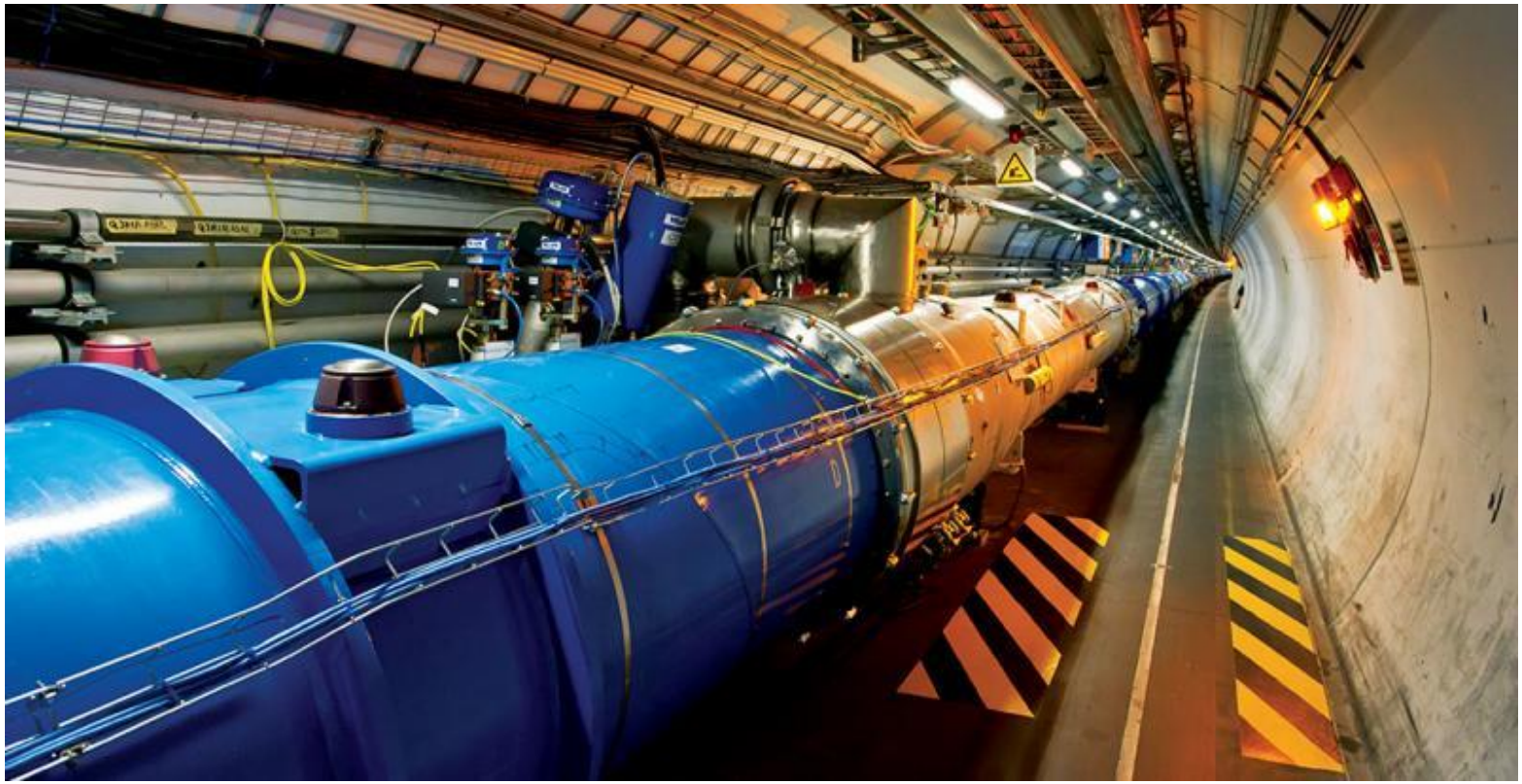


High DR ADC for LHC

Sarthak Kalani

Last updated: 05/12/17

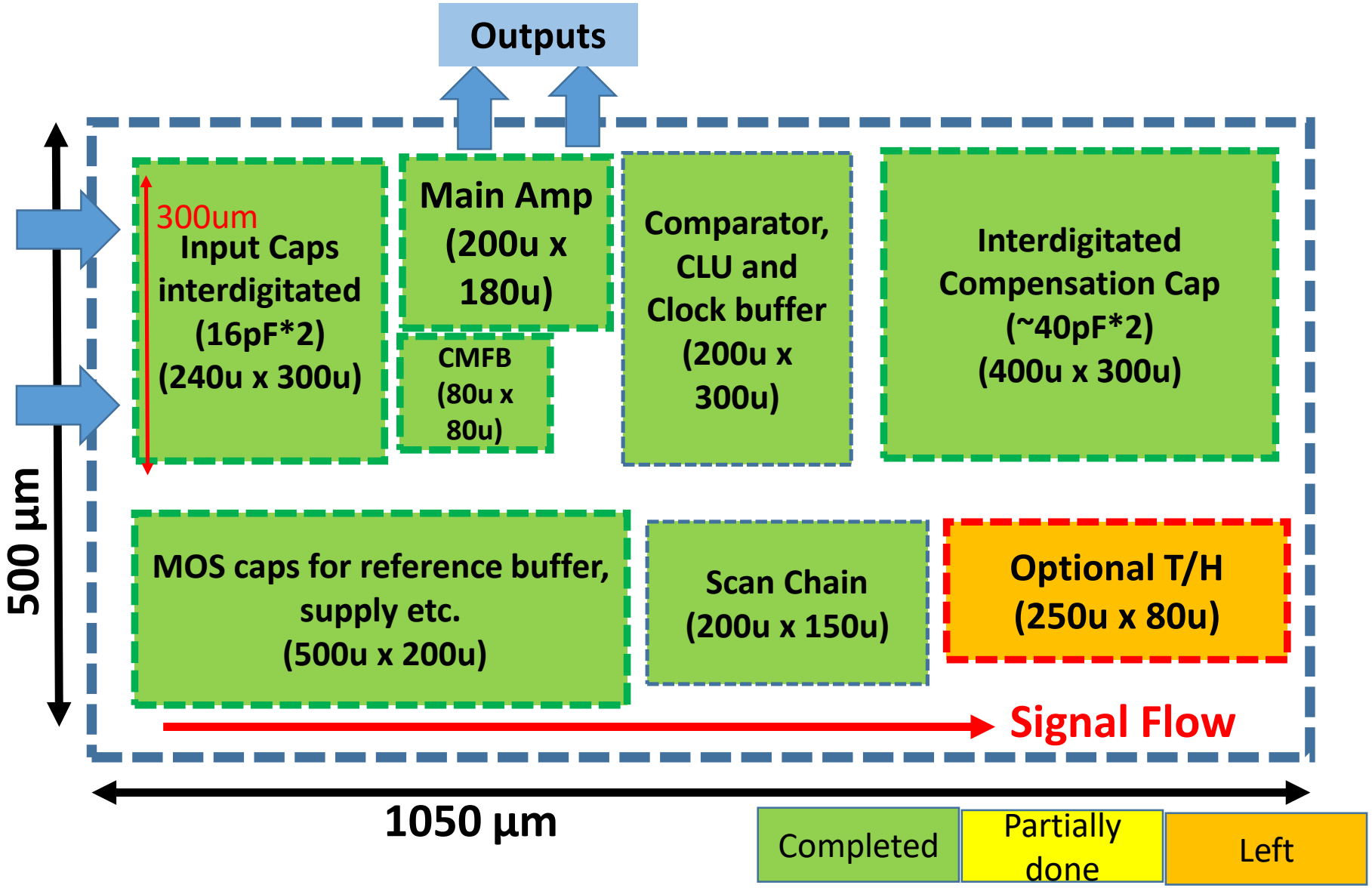
COLUMBIA UNIVERSITY
IN THE CITY OF NEW YORK

Columbia Integrated Systems Laboratory

Status update

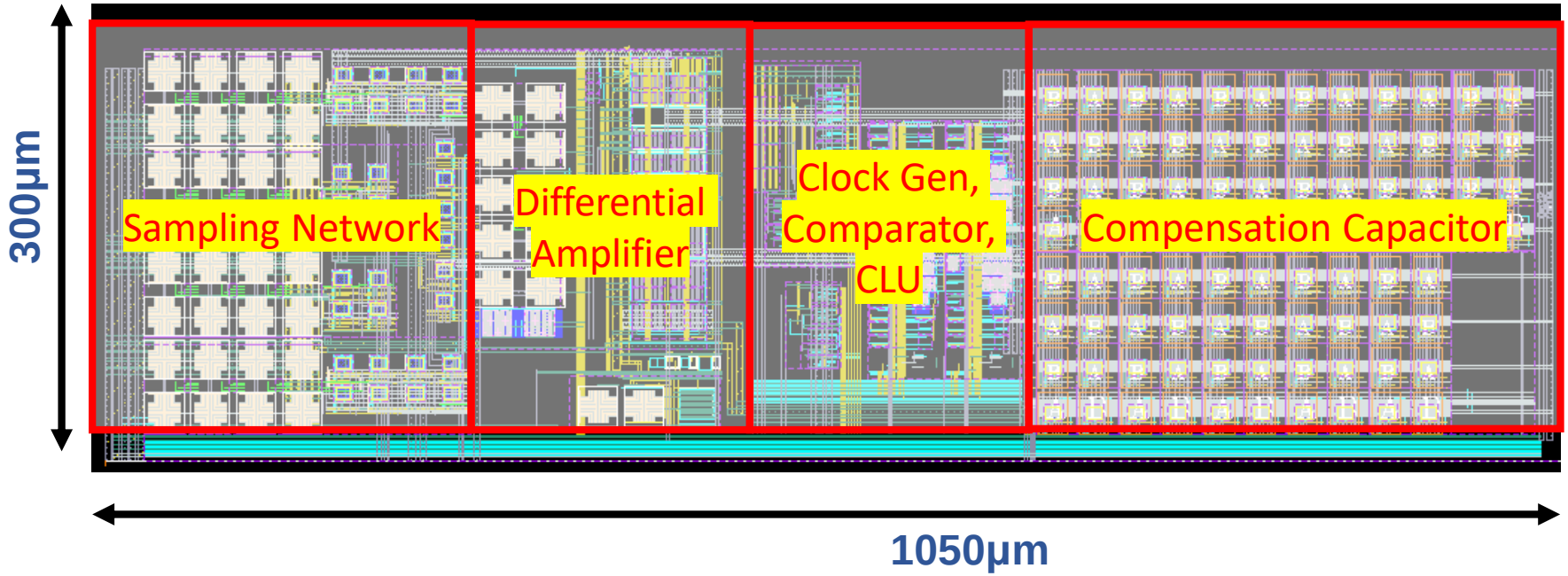
- DRE layout done
- Top level integration with chip: Almost done
- Only metal fill is left
- Simulations
  - Currently at schematic level
    - CERN requirements are met across process corners
    - Best performance
      - Met at TT27, not being met currently across corners.
      - Distortion is the main issue…

DRE block layout scheme



Channel area: 950 µm x 300 µm, Active area: 950 µm x 500 µm

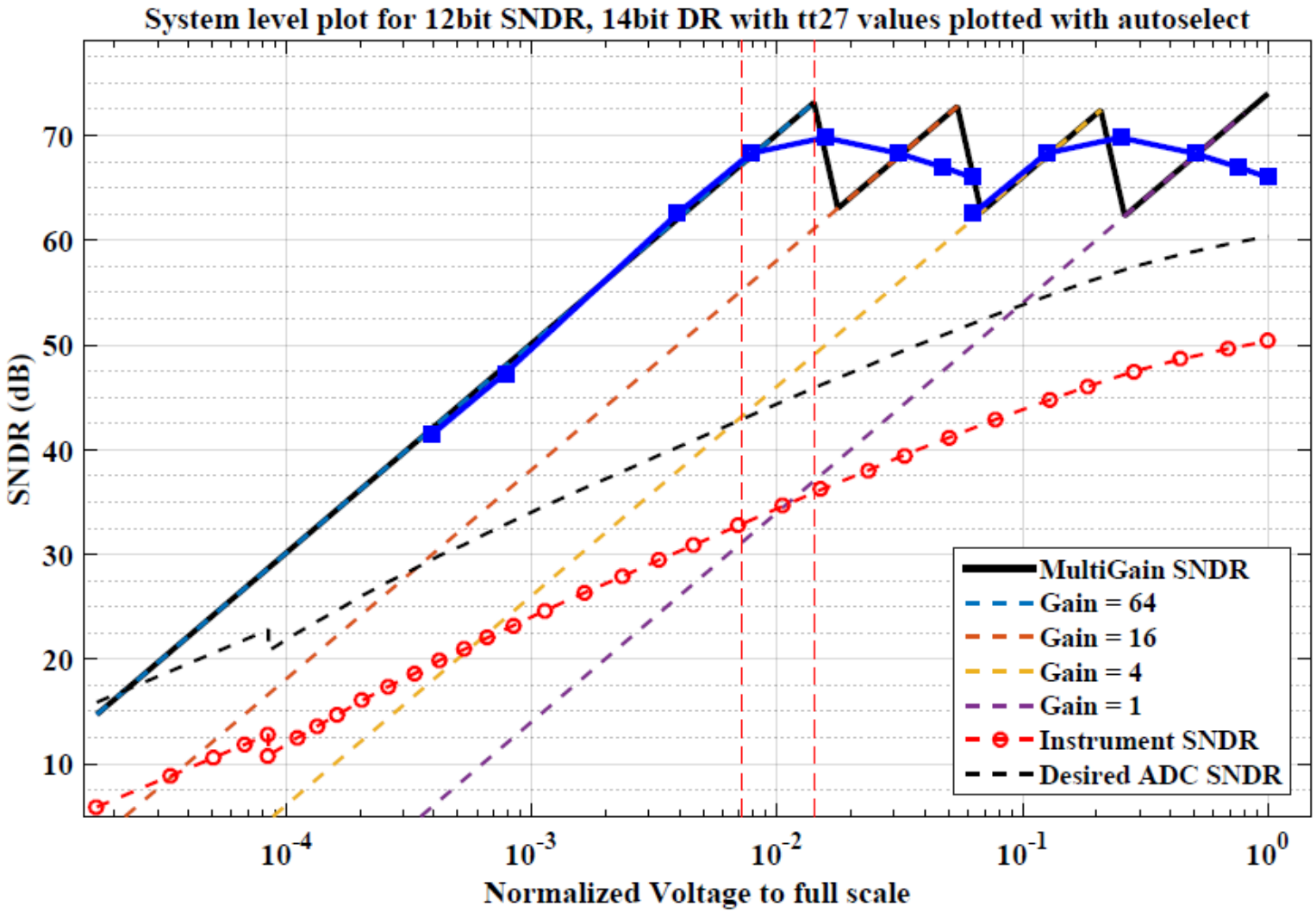
Layout Status update



- Integration complete with Scan Chain, serializer, pads
- Waiting for SAR to complete. 3 pins to be connected.
- Metal fill to be done.

CERN requirements

- Just for reference. No results to be inferred here.



Simulation Results

- Simulation done at DRE block schematic level, with bondwires (4nH), outputs taken externally, loading with 2pF (single ended).
- Autoselect used in all simulations. Vfs = 1.6Vpp assumed. I = 12mA to 21mA

Input Freq	Input Amp (diffpp)	Ideal SNDR (for current architecture)	CERN SNDR required (including 10dB margin)	tt27	ss27	ff27	fs27	sf27
4.844M	0.2V	67dB	>52dB	66.76	59.62	65.99	66.97	66.78
	0.4V	73dB	>54dB	66.51	62.41	64.2	62.25	68.65
	0.8V	73dB	>58dB	68.88	65.55	53.28	63.52	70.57
	1.6V	73dB	>60dB	73.85	69.8	60.04	70.55	74.22
19.84M	0.2V	67dB	>52dB	66.86	57.27	66.01	66.62	66.42
	0.4V	73dB	>54dB	70.32	59.7	66.65	69.11	68.65
	0.8V	73dB	>58dB	67.77	66	53.91	63.44	70.03
	1.6V	73dB	>60dB	66.44	60.04	63.15	66.96	70

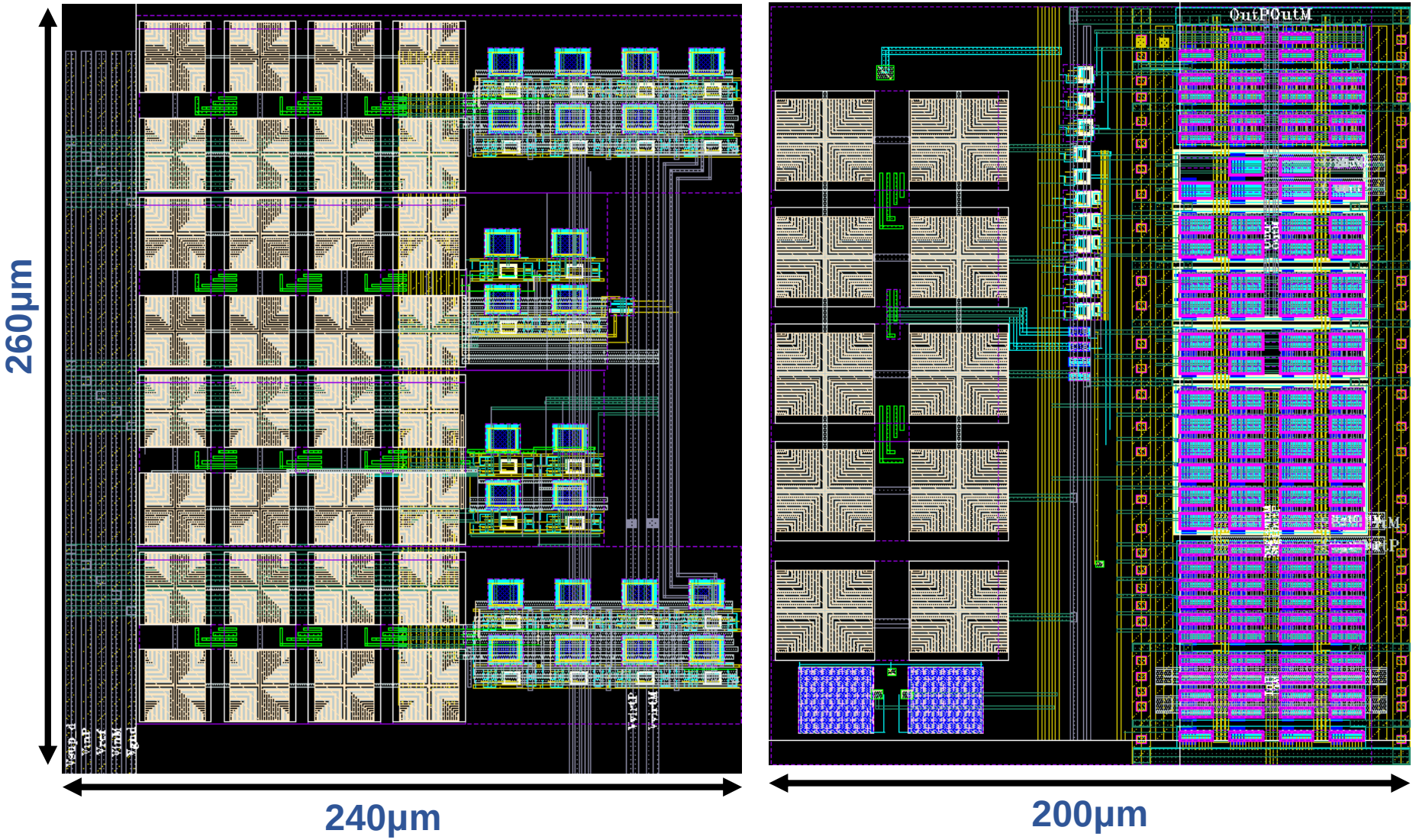
(Self note: Sims: I13 to I16, 30_pcb_sim_v2_woParametric) (Coloring from CERN perspective)

Next steps

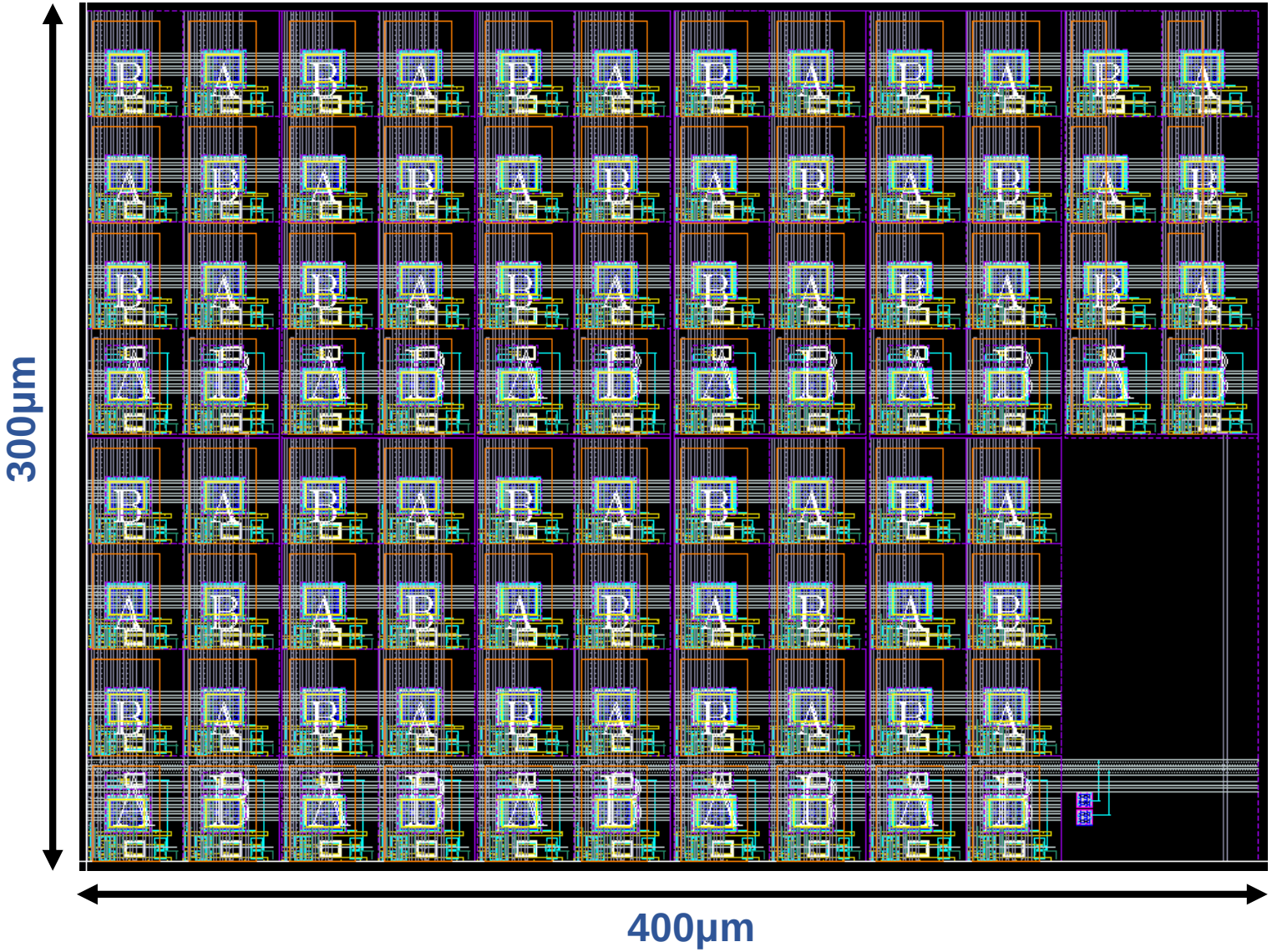
- Working on a better version of Amplifier
- If I get better results for Aplifier by Monday (May 15th), will layout by May 18th, and verify by May 24th
- If not, will send the current version for tapeout.
- Meanwhile, simulations continue…

Backup Slides

Sampling network and Differential Amplifier



Miller Compensation Capacitor



Clock Generator, Comparator & CLU